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U.S. Patent and Trademark Office, Group Art Unit 2818**Fax#:** +1 (571) 273-1796**FROM:** Brian Wichner, Reg. No. 52,359**Date:** Friday, May 06, 2005

Number of pages (including this one): 1

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**REMARKS:** Our Docket No. 8750-045  
U.S. Patent Application No. 10/632,700, Art Unit: 2818

Examiner Mai-Huong Tran:

As we discussed yesterday by phone, please find the enclosed draft amendment of claim 26. This is for your review prior to our scheduled phone interview at 1:30 pm (EST) Wednesday, May 11.

Regarding the draft amendment of claim #26, the applicant wishes to further distinguish claim 26 from the Ishio reference by including language that a pad is between the two chips. Ishio does teach this. Ishio only shows, in FIG. 1, pads (2) on a substrate (1) where the pads are not in a region between the two chips (substrates 1 and 5).

Regarding the existing claims 1-25 and the enclosed draft amendment of claim 26, the term "tape" and its meaning is not taught by the Ishio reference. Specifically, Ishio teaches the first insulating film 3 (FIG. 1) is made of a SiN film and a polyimide film (Col. 5, line 65). These materials may not be considered a "tape", as recited in the claims of the instant application because they are materials that are grown on a substrate, whereas a "tape" is a distinct layer that is not grown on the surface to which it is applied.

Please call at (503) 222-3613 if you have any questions.

I appreciate your attention to this matter and look forward to discussing this with you further.

Should you need any additional information, please feel free to contact me.

Best regards,

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## DRAFT

For convenience of the phone interview for May 11, 2005, only one draft amendment of the claims is submitted for Examiner review.

26. (Draft amendment) A multi-chip module comprising:
- a substrate having a plurality of interconnections formed on a top surface thereof;
  - a lowest chip and at least one top chip sequentially stacked on the top surface, the top chip having an insulating tape attached to a backside thereof, the lowest chip and the top chip each having pads formed thereon, at least one pad being between the lowest chip and the top chip;
  - an insulator interposed between the chips, the insulator exposing the at least one ~~the pads;~~ and
  - a first ~~group of bonding wires connecting~~ the at least one pad ~~the pads of the lowest chip with a first group of interconnection~~[[s]] on the substrate,
- wherein the insulating tape attached to the backside of the top chip insulates the first ~~group of bonding wire~~[[s]] from directly contacting the top chip.

DRAFT